

## REMARKS

Claims 1-17 remain pending in the application.

Claims 1, 3-5 and 17 stand rejected under 35 U.S.C. 102(b) as being anticipated by Lampaert et al. (U.S. Patent Application 2002/0188920) (Lampaert).

Regarding the rejection of Claims 1 and 17, Applicants respectfully traverse the stated rejection for the following reasons:

The Office Action states that Lampaert teaches in Paragraph 0055 and 0057, Fig. 6, of his patent application the step:

“identifying transistors in a sub-circuit configuration that includes respective interconnections linked to each of said transistors;”

Applicants submit that Lampaert teaches in steps 806 and 804 (FIG. 8) ‘predicting the electrical behavior of the RF MOSFET including internal parasitics’. The teaching Lampaert is unrelated to “identifying transistors...” nor to “performing a physical verification”.

Moreover, in Paragraph 0057, Lampaert teaches “RF MOSFET parameter Wf...” which describes a number of parameters based on knowing the target is a MOSFET transistor and, then, based on the extracted parameters it calculates the parasitic elements electrical parameter values, e.g., the parasitic capacitance.

Thus, Lampaert patent teaches using MOSFET extracted parameters to optimize a design process. In contrast, Applicants teach in claims 1 and 17 “...identifying transistors in a sub-circuit configuration ...” in order to determine whether the target is a transistor or some other electrical elements. If it is determined as a transistor, the program will perform transistor parameter extraction. Otherwise, it will perform another electrical

element extraction based on what element it has recognized (see Claim 15). Applicant's teaching is therefore a method for verifying the layout and determine its schematic design correlation. Lampaert, on the other hand, teaches away from "checking the layout of a design against its schematic (LVS) representation" and "how to actually perform this LVS check" as stated in paragraph [0066] regarding DRC (design rule check) and LVS as taught in step [808] of Lampaert's application publication.

In view of the foregoing, it is not possible for Lampaert to perform a sub-circuit based LVS because, among others, he cannot distinguish a multi-fingered FET from a multi-fingered MOS capacitor. In addition, Lampaert does not teach nor suggest how to apportion a sub-circuit for layout extraction and verification. Therefore, our claim #1 and #17, which are to claim a method of performing a physical verification of the sub-circuit based layout, are substantially different from [Lampaert] patent.

Regarding the Fig. 6 of Lampart's patent application, it represents a typical and well known multi-finger MOSFET transistor layout of a design of the art and adds nothing to the teaching of Lampaert when compared to that of the Applicants.

The Office Action further states that Lampaert teaches:

"measuring parameters of each of said sub-circuits [paragraphs 0055-0057 – the predictive RF MOSFET layout is an extraction] of [US Patent Application Publication 2002/0188920 by Lampaert]."

Applicants contend that Paragraph 0055 of Lampaert cited reference predicts the electrical behavior of the RF MOSFET including internal parasitics using step 804, 806, and subcircuit model 300, which enables the designers to design a circuit that incorporates an RF MOSFET's internal parasitics prior to RF MOSFET layout generation. Applicants submit that sub-circuit model 300 only comprises electrical element, and none of the element electrical values can be measured from a circuit layout.

Applicants contend further that Paragraph 0057 of Lampaert cited patent teaches “measuring parameters ...”. Applicants submit that they teach in their invention “identifying – measuring – verifying” while the referred patent is restricted to only “knowing it is a MOSFET and extracting the parameters”. Therefore, in view of this limitation, it is not possible for Lampaert to teach the remaining step of Claim 1 and 17, of the present application.

Regarding the assertion that Lampaert teaches “comparing the measured parameters of each of said sub-circuits ... [fig. 8, element 810] of U.S. Patent Application Publication 2002/0188920 by Lampaert].. Applicants submit that Fig. 8, element 810 is one flow chart element of a general integrated circuit design. Element 810 does identify an electrical element, extract geometric parameters, and verifies the layout with circuit schematic design to enhance circuit design confidence.

Regarding the assertion that Lampaert teaches “determining if all of said comparisons returns a correct correlation ... [0066] of US Patent Application Publication 2002/0188920 by Lampaert, Applicants submit that paragraph [0066] is a textbook description of a DRC and an LVS. Lampaert limits his teaching to DRCs (design rule checks) and LVS. This is not, as explained *supra*, related to Applicants’ teaching.

Regarding Claims, 3, 4, 5 and 10, Applicants submit that they are all dependent claims of Claim 1. Since Applicants believe that Lampaert does not teach the same invention as Applicants, then, neither will all the claims that are dependent on Claim 1.

In view of the foregoing, Applicants believe that all the rejected claims are free of rejection under 35 U.S.C. 102(b) over Lampaert, and respectfully request that the Examiner reconsider and withdraw the rejection of the stated claims based thereon.

Claims 11, 14-16 stand rejected under 35 U.S.C. 102(b) as being anticipated by Li (US Patent Application Publication 2004/0025125).

The Office Action states that Li teaches the invention as claimed. Applicants respectfully traverse this assertion for the following reasons:

The Office action states that Li teaches “.... a method for creating a device layout comprising the steps of: ... geometric parameters [paragraph 0006, paragraph 0008]”

Regarding the rejection of Claim 11, Applicants contend that Paragraph 0006 and 0008 describe the layout design process and layout extraction process. Applicants teach “providing device model parameters...” especially a sub-circuit based device model which supports a complex layout extraction with a list of sub-circuit geometric parameters. This key step is not taught nor suggested by Li., in addition to similar arguments already provided supra when addressing the rejection of claims 1 and 17 in view of Lampaert.

The Office Action further states that Li teaches “providing specific marker shapes to define the device layout geometric parameters ... [paragraph 0092]”

Applicants contend that the “marker geometries” in paragraph 0092 refers to a “DRC error marker geometries generated by an electronic design automation (EAD) tool...” It is used for erroneous edge segments in the DRC process. The marker shapes in claim 11 is a design layer/shape, and a component of a sub-circuit device layout needed for layout verification. Thus, the two markers referred by Li and the markers taught by Applicants are totally unrelated to each other. Applicants submit that if the markers referred by Li were utilized in the present application, such markers would have been totally useless to satisfy the execution of the remaining steps taught in the independent claim.

Regarding the rejection of Claim 14 (dependent on claim 11), the Office Action recites: “wherein said devices are selected from the group consisting of bipolar junction transistors (BJT), hetero-junction bipolar transistors (HBT), and compounded semiconductor transistors [paragraph 0008 – transistors, which includes BJT, HBT, and/or compounded semiconductor transistors]. Applicants contend that in addition to

Claim 14 being dependent on claim 11, in Paragraph 0008 – transistors, which include BJT, HBT, and/or compounded semiconductor transistors is to cover common sense layout extraction for all other types of transistors.

Applicants submit that claim 14 teaches a sub-circuit based layout extraction and verification, which as explained earlier is not possible to achieve with markers taught by Li.

The Office Action further recites for claim 15, “wherein further marker shapes are added to non-FET devices ... [paragraph 0043].”

Applicants contend that Paragraph 0043 utilizes a marker layer to optimize the layout design, such as optimizing ground and power line wiring. The marker layer taught by the Applicants provides layout extraction and verification assistance.

The Office Action states that in claim 16, “non-FET devices are selected from the group consisting of integrated on-chip inductors ... [paragraph 0039].

Applicants submit that Paragraph 0039 teaches a non-orthogonal geometries treatment whereas Claim 16 teaches a sub-circuit based extraction and verification for the non-FET devices, such as resistor and capacitor, all of which are not taught nor suggested by Li.

Thus, Applicants believe that all the rejected claims are free of rejection under 35 U.S.C. 102(b) over Li., and respectfully request that the Examiner reconsider and withdraw the rejection of the stated claims based thereon.

In view of the foregoing arguments, Applicants respectfully request that all the rejections and objections to this application be reconsidered and withdrawn and that the Examiner pass all the pending claims to issue.

Should the Examiner have any suggestions pertinent to the allowance of this application, the Examiner is encouraged to contact Applicants' undersigned representative.

Respectfully submitted,

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